forming a data wire including a source electrode, a drain electrode and a data line connected to the source electrode on the semiconductor pattern so that a portion of the semiconductor pattern between the source electrode and the drain electrode are exposed;

forming color filters made of photosensitive material, the filters covering the data wire, directly contacting the exposed portion of the semiconductor pattern, and having a first contact hole; and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters.

34. (Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on an ohmic contact layer;

forming red, green, and blue color filters, said filters made of photosensitive material and covering the data wire and having a first contact hole;

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters; and

forming a passivation layer covering a color filter before forming red, green, and blue color filters, the passivation layer being made of photosensitive transparent organic material having a good planarization property, wherein

the red, green, and blue color filters, and the passivation layer are patterned through only exposure and development to form the first contact hole,

the gate wire further includes a gate pad that is connected to and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to and receives a signal from an external circuit, and the color filter, the passivation layer, and the gate insulating

layer have a second contact hole and a third contact hole respectively exposing the gate pad and the data pad, and

further comprising a step of forming a redundant gate pad and a redundant data pad that are made of the same layer as the pixel electrode and respectively connected to the gate pad and the data pad through the second contact hole and the third contact hole.

37. (Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on an ohmic contact layer;

forming red, green, and blue color filters, said filters made of photosensitive material and covering the data wire and having a first contact hole; and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters, wherein

the gate wire or the data wire is made of photosensitive conductive material, and

the gate wire and the data wire are patterned through only exposure and development, and are made of Ag paste or copper organic metal that includes photoresist.

38. (Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on an ohmic contact layer;

forming red, green, and blue color filters, said filters made of photosensitive material and covering the data wire and having a first contact hole; and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters,

wherein the source electrode and the drain electrode are separated by a photolithography process using a data wire pattern, and the data wire pattern has a first portion having a first thickness and is at least located between the source electrode and the drain electrode, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

46. (Amended) A thin film transistor array panel for a liquid crystal display, comprising:

a gate wire including a gate line and a gate electrode connected to the gate line, and formed on an insulating substrate;

a gate insulating layer covering the gate electrode;

a semiconductor pattern formed on the gate insulating layer;

a data wire including a source electrode and a drain electrode, and a data line connected to the source electrode;

a passivation layer covering the data wire and having a first contact hole exposing the drain electrode; and

a pixel electrode connected to the drain electrode through the first contact hole,

wherein the gate wire or the data wire are made of photodefinable conductive material.

Please add claims 64-74 as follows:

64. (New) A thin film transistor array panel for a liquid crystal display, comprising:

a plurality of gate lines formed on an insulating substrate;

a gate insulating layer covering the gate lines;

a plurality of data lines intersecting the gate lines;

an array of thin film transistors, each transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, and a drain electrode;

a plurality of color filters formed over the gate insulating layer, the color filters overlapping the data lines at least in part; and

a plurality of pixel electrodes formed on the color filters, each pixel electrode electrically connected to the drain electrode.

65. (New) The thin film transistor array panel fo claim 64, wherein each of the pixel electrodes overlaps at least one of the data lines a least in part.

66. (New) The thin film transistor array panel of claim 64, wherein the data line comprises an amorphous silicon layer, an ohmic contact layer and a metal layer.

67. (New) The thin film transistor array panel of claim 64, further comprising a storage electrode made of the same layer as the gate lines.

68. (New) The thin film transistor array panel of claim 67, further comprising a conductor pattern overlapping the storage electrode, the conductor pattern made of the same layer as the data lines.

69. (New) The thin film transistor array panel of claim 64, wherein adjacent two of the color filters overlap each other at least in part.

70. (New) The thin film transistor array panel of claim 64, further comprising an insulating layer interposed between the color filters and the pixel electrodes.

71. (New) A thin film transistor array panel for liquid crystal display, comprising

a plurality of gate lines formed on an insulating substrate;

a first insulating layer covering the gate lines;

a plurality of data lines intersecting the gate lines, each data line including an amorphous silicon layer, an ohmic contact layer and a metal layer;

an array of thin film transistors, each transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, and a drain electrode;

a second insulating layer formed at least on the data lines, the second insulating layer contacting a portion of the amorphous silicon layer exposed between the source electrode and the drain electrode; and

a plurality of pixel electrodes formed on the second insulating layer, each pixel electrode electrically connected to the drain electrode.

72. (New) The thin film transistor array panel of claim 71, wherein each of the pixel electrodes overlaps at least one of the data lines at least in part.

73. (New) The thin film transistor array panel of claim 64, further comprising a storage electrode made of the same layer as the gate lines.

74. (New) The thin film transistor array panel of claim 73, further comprising a conductor pattern overlapping the storage electrode, the conductor pattern made of the same layer as the data lines.

REMARKS

Claims 1-12, 29-48 and 64-74 are currently pending in the application. By this amendment, claims 29, 34, 37, 38 and 46 are amended and claims 13-28 and 50-63 are canceled without prejudice or disclaimer. Claims 64-74 are also added for the Examiner's consideration. Attached hereto is a separate sheet entitled "Marked-Up Copy of Claims" showing a marked up copy of the amended claims. Support for the amendment(s) is provided in at least Figures 3 and